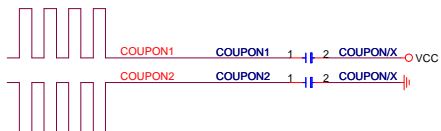
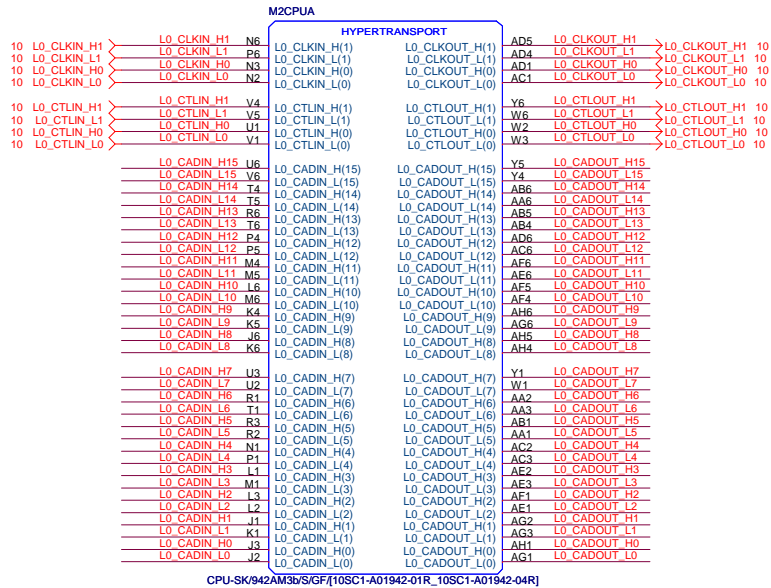
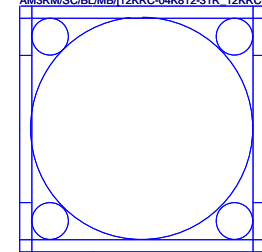


CPU\_VDD\_RUN = VCORE  
 CPU\_VDDA\_RUN = VDDA25  
 VLDT\_RUN = VCC12\_HT  
 CPU\_VDDIO\_SUS = DDR15V  
 CPU\_VDDR = CPU\_VDDR12

VLDT\_A = VCC12\_HT  
 VLDT\_B = HT12B

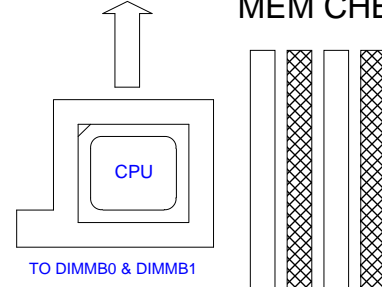
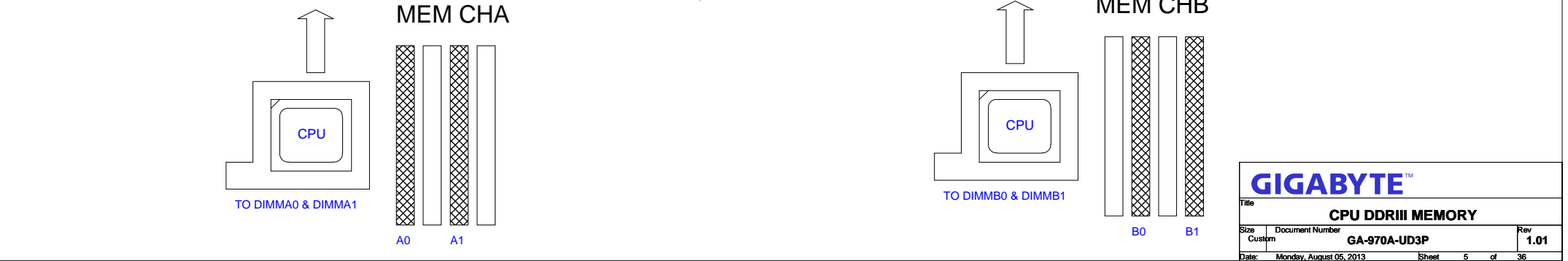


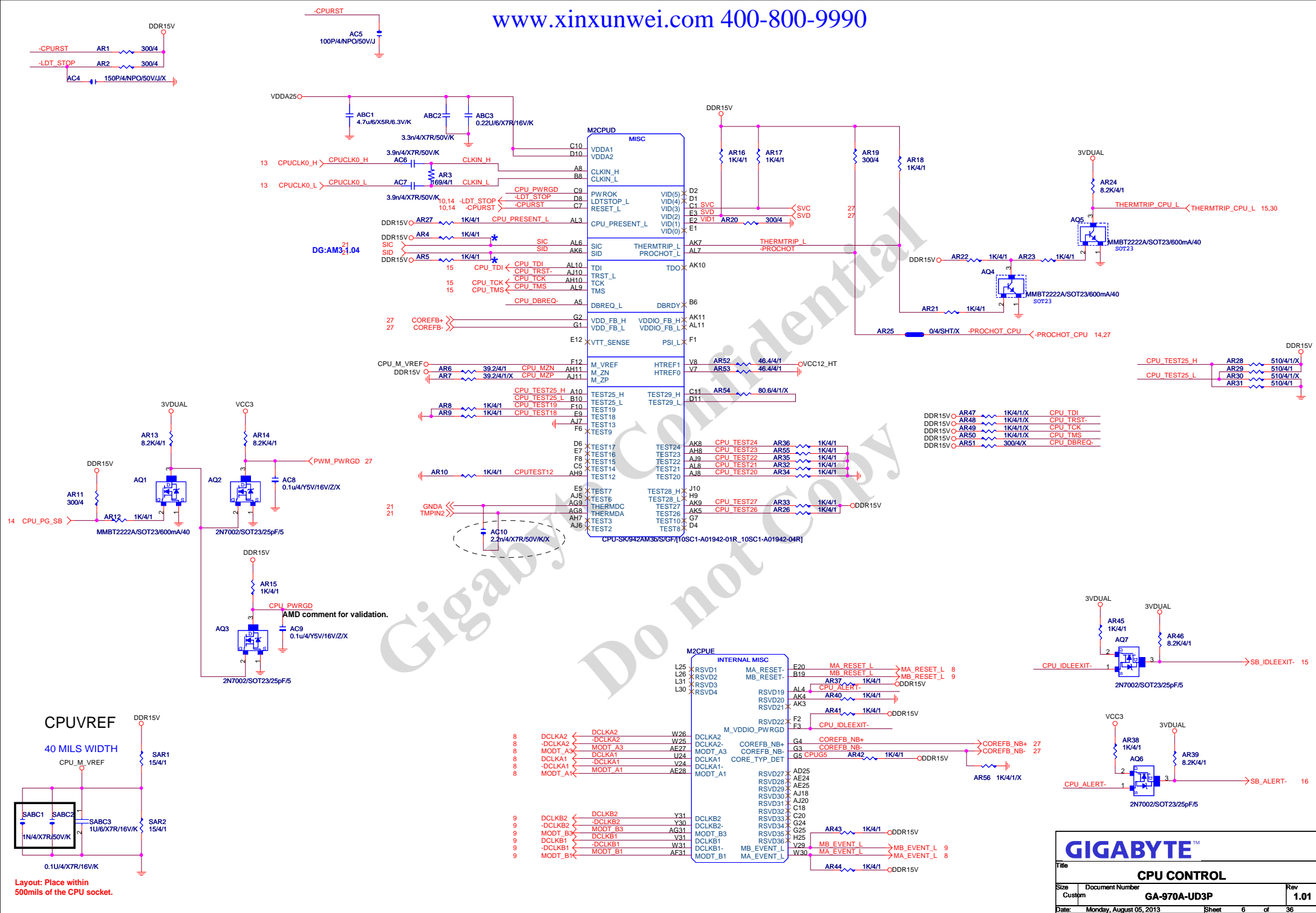
M2CPU  
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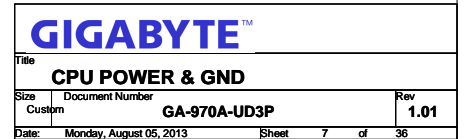


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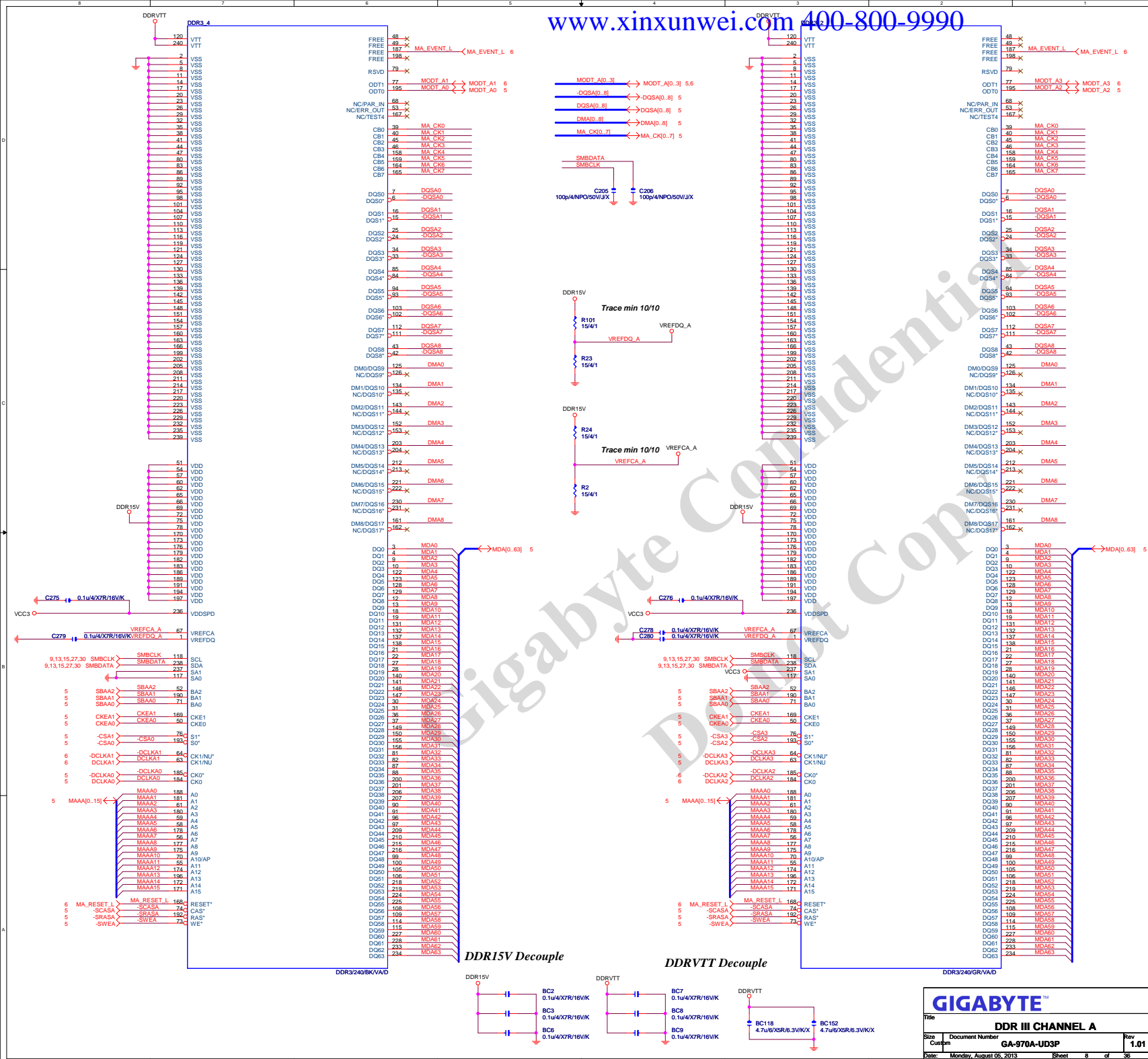
Title			
CPU HYPER TRANSPORT			
Size	Document Number	Rev	
Custom	GA-970A-UD3P	1.01	
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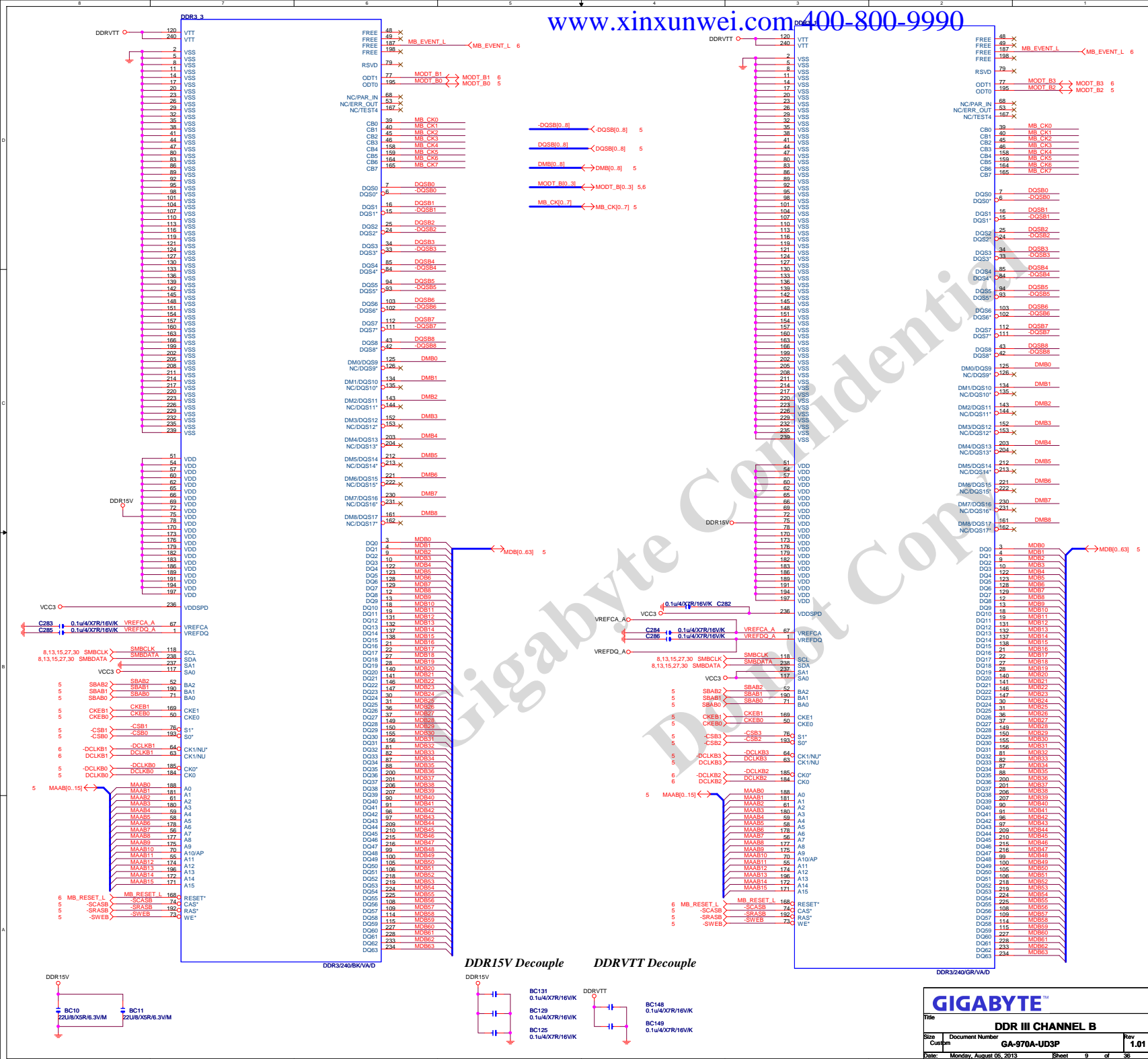












U3A

## PART 1/5

## HYPERTRANSPORT IF

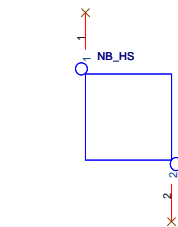
RX980/BGA692

L0\_CADIN\_L[0..15] &lt;L0\_CADIN\_L[0..15] 4

L0\_CADIN\_H[0..15] &lt;L0\_CADIN\_H[0..15] 4

L0\_CADOUT\_L[0..15] &lt;L0\_CADOUT\_L[0..15] 4

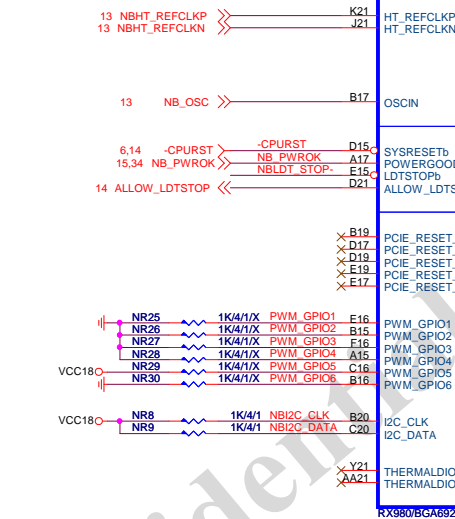
L0\_CADOUT\_H[0..15] &lt;L0\_CADOUT\_H[0..15] 4



NB\_HS[12SP2-SA0702-01R\_12SP2-SA0702-02R]

HT_RXCAD15P	N23	L0_CADIN_H15
HT_RXCAD15N	N24	L0_CADIN_L15
HT_RXCAD14P	M24	L0_CADIN_H14
HT_RXCAD14N	M25	L0_CADIN_L14
HT_RXCAD13P	L23	L0_CADIN_H13
HT_RXCAD13N	L24	L0_CADIN_L13
HT_RXCAD12P	K24	L0_CADIN_H12
HT_RXCAD12N	K25	L0_CADIN_L12
HT_RXCAD11P	H24	L0_CADIN_H11
HT_RXCAD11N	H25	L0_CADIN_L11
HT_RXCAD10P	G24	L0_CADIN_H10
HT_RXCAD10N	G25	L0_CADIN_L10
HT_RXCAD9P	F24	L0_CADIN_H9
HT_RXCAD9N	F25	L0_CADIN_L9
HT_RXCAD8P	E24	L0_CADIN_H8
HT_RXCAD8N	E25	L0_CADIN_L8
HT_RXCAD7P	N26	L0_CADIN_H7
HT_RXCAD7N	N27	L0_CADIN_L7
HT_RXCAD6P	M27	L0_CADIN_H6
HT_RXCAD6N	M28	L0_CADIN_L6
HT_RXCAD5P	L26	L0_CADIN_H5
HT_RXCAD5N	L27	L0_CADIN_L5
HT_RXCAD4P	K27	L0_CADIN_H4
HT_RXCAD4N	K28	L0_CADIN_L4
HT_RXCAD3P	H27	L0_CADIN_H3
HT_RXCAD3N	H28	L0_CADIN_L3
HT_RXCAD2P	G27	L0_CADIN_H2
HT_RXCAD2N	G28	L0_CADIN_L2
HT_RXCAD1P	F27	L0_CADIN_H1
HT_RXCAD1N	F28	L0_CADIN_L1
HT_RXCAD0P	E26	L0_CADIN_H0
HT_RXCAD0N	E27	L0_CADIN_L0

HT_RXCLK1P	J23	L0_CLKIN_H1
HT_RXCLK1N	J24	L0_CLKIN_L1
HT_RXCLK0P	J26	L0_CLKIN_H0
HT_RXCLK0N	J27	L0_CLKIN_L0
HT_RXCTL1P	P24	L0_CTLIN_H1
HT_RXCTL1N	P25	L0_CTLIN_L1
HT_RXCTL0P	P27	L0_CTLIN_H0
HT_RXCTL0N	P28	L0_CTLIN_L0
HT_TXCALP	D28	HT_TXCALP NR1
HT_TXCALN	D27	HT_TXCALN

PART 3/5  
CLOCKS

## PM

## MISC.

## STRP\_DATA

GPP1\_REFCLKP  
GPP1\_REFCLKN  
GPP2\_REFCLKP  
GPP2\_REFCLKN  
GPP3\_REFCLKP  
GPP3\_REFCLKN

J8 NBGFX\_CLKP 13  
H8 NBGFX\_CLKN 13  
V8 NBGFX1\_CLKP 13  
U8 NBGFX1\_CLKN 13  
AA15 NBGPP\_CLKP 13  
AA14 NBGPP\_CLKN 13

DFT\_GPIO0/NM#  
DFT\_GPIO1  
DFT\_GPIO2  
DFT\_GPIO3  
DFT\_GPIO4  
DFT\_GPIO5/SYNCFLOODIN#

DBG\_GPIO0/SERR\_FATA#  
DBG\_GPIO1/SIC  
DBG\_GPIO2/SID  
DBG\_GPIO3/NON\_FATA\_CORR#

## STRP\_DATA

## TESTMODE

## DFT\_GPIO5: STRAP\_DEBUG\_BUS\_GPIO\_ENABLEB

Enables the Test Debug Bus using GPIO.  
1 : Disable ( Can still be enabled using nbcfg register access)  
0 : Enable

## DFT\_GPIO[4:2]: STRAP\_PCIE\_GPP\_CFG[2:0]

These pin straps are used to configure PCI-E GPP mode.

GPIO4:3:2  
000 : 4:2:4 B  
001 : 4:1:1:4 C  
010 : 1:1:1:1:1:1:4 L (Hardware Default)  
011 : 2:1:1:1:1:1:4 E  
100 : 2:2:1:1:4 K  
101 : 2:2:2:4 C2  
110 : Hardware default (mode L) or EEPROM  
111 : Hardware default (mode L) or EEPROM  
101 : 01100  
111 : 01011

## DFT\_GPIO1: LOAD\_EEPROM\_STRAPS

Selects Loading of STRAPS from EPROM

1 : Bypass the loading of EEPROM straps and use Hardware Default Values  
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

## DFT\_GPIO0: STRAP\_DEBUG\_BUS\_PCIE\_ENABLEB

Enables the Test Debug Bus using PCIE bus  
1 : Disable ( Can still be enabled using nbcfg register access )  
0 : Enable

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Title RS780 HT-LINK V/F

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U3B

PART 2/5

EXP A\_RXP15 N6  
EXP A\_RXN15 N5  
EXP A\_RXP14 M5  
EXP A\_RXN14 M4  
EXP A\_RXP13 L6  
EXP A\_RXN13 L5  
EXP A\_RXP12 K5  
EXP A\_RXN12 K4  
EXP A\_RXP11 J6  
EXP A\_RXN11 J5  
EXP A\_RXP10 H4  
EXP A\_RXN10 H4  
EXP A\_RXP9 G6  
EXP A\_RXN9 G5  
EXP A\_RXP8 F5  
EXP A\_RXN8 F4  
EXP A\_RXP7 D2  
EXP A\_RXN7 D1  
EXP A\_RXP6 B5  
EXP A\_RXN6 C6  
EXP A\_RXP5 D6  
EXP A\_RXN5 E6  
EXP A\_RXP4 E7  
EXP A\_RXN4 F7  
EXP A\_RXP3 F8  
EXP A\_RXN3 E8  
EXP A\_RXP2 E9  
EXP A\_RXN2 F9  
EXP A\_RXP1 D10  
EXP A\_RXN1 E10  
EXP A\_RXP0 E11  
EXP A\_RXN0 F11

GPP1\_RX15P  
GPP1\_RX15N  
GPP1\_RX14P  
GPP1\_RX14N  
GPP1\_RX13P  
GPP1\_RX13N  
GPP1\_RX12P  
GPP1\_RX12N  
GPP1\_RX11P  
GPP1\_RX11N  
GPP1\_RX10P  
GPP1\_RX10N  
GPP1\_RX9P  
GPP1\_RX9N  
GPP1\_RX8P  
GPP1\_RX8N  
GPP1\_RX7P  
GPP1\_RX7N  
GPP1\_RX6P  
GPP1\_RX6N  
GPP1\_RX5P  
GPP1\_RX5N  
GPP1\_RX4P  
GPP1\_RX4N  
GPP1\_RX3P  
GPP1\_RX3N  
GPP1\_RX2P  
GPP1\_RX2N  
GPP1\_RX1P  
GPP1\_RX1N  
GPP1\_RX0P  
GPP1\_RX0N

PCIE GPP1

GPP2\_TX15P  
GPP2\_TX15N  
GPP2\_TX14P  
GPP2\_TX14N  
GPP2\_TX13P  
GPP2\_TX13N  
GPP2\_TX12P  
GPP2\_TX12N  
GPP2\_TX11P  
GPP2\_TX11N  
GPP2\_TX10P  
GPP2\_TX10N  
GPP2\_TX9P  
GPP2\_TX9N  
GPP2\_TX8P  
GPP2\_TX8N  
GPP2\_TX7P  
GPP2\_TX7N  
GPP2\_TX6P  
GPP2\_TX6N  
GPP2\_TX5P  
GPP2\_TX5N  
GPP2\_TX4P  
GPP2\_TX4N  
GPP2\_TX3P  
GPP2\_TX3N  
GPP2\_TX2P  
GPP2\_TX2N  
GPP2\_TX1P  
GPP2\_TX1N  
GPP2\_TX0P  
GPP2\_TX0N

N3  
N2  
M1  
L3  
L2  
K2  
K1  
J3  
J2  
H2  
H1  
G3  
G2  
F2  
F1  
E3  
E2  
A4  
B4  
A6  
B6  
B7  
C7  
A8  
B8  
C9  
A10  
B10  
C11

EXP A\_TXP15  
EXP A\_TXN15  
EXP A\_TXP14  
EXP A\_TXN14  
EXP A\_TXP13  
EXP A\_TXN13  
EXP A\_TXP12  
EXP A\_TXN12  
EXP A\_TXP11  
EXP A\_TXN11  
EXP A\_TXP10  
EXP A\_TXN10  
EXP A\_TXP9  
EXP A\_TXN9  
EXP A\_TXP8  
EXP A\_TXN8  
EXP A\_TXP7  
EXP A\_TXN7  
EXP A\_TXP6  
EXP A\_TXN6  
EXP A\_TXP5  
EXP A\_TXN5  
EXP A\_TXP4  
EXP A\_TXN4  
EXP A\_TXP3  
EXP A\_TXN3  
EXP A\_TXP2  
EXP A\_TXN2  
EXP A\_TXP1  
EXP A\_TXN1  
EXP A\_TXP0  
EXP A\_TXN0

AC9  
AD9  
AE8  
AC7  
AD7  
AD6  
AE6  
AE5  
AG5  
AF2  
AD2  
AD1  
AB5  
AB4  
AA6  
AA5  
Y5  
Y4  
W6  
W5  
V5  
V4  
U6  
U5  
T5  
T4  
R6  
R5  
P5  
P4

GPP2\_RX15P  
GPP2\_RX15N  
GPP2\_RX14P  
GPP2\_RX14N  
GPP2\_RX13P  
GPP2\_RX13N  
GPP2\_RX12P  
GPP2\_RX12N  
GPP2\_RX11P  
GPP2\_RX11N  
GPP2\_RX10P  
GPP2\_RX10N  
GPP2\_RX9P  
GPP2\_RX9N  
GPP2\_RX8P  
GPP2\_RX8N  
GPP2\_RX7P  
GPP2\_RX7N  
GPP2\_RX6P  
GPP2\_RX6N  
GPP2\_RX5P  
GPP2\_RX5N  
GPP2\_RX4P  
GPP2\_RX4N  
GPP2\_RX3P  
GPP2\_RX3N  
GPP2\_RX2P  
GPP2\_RX2N  
GPP2\_RX1P  
GPP2\_RX1N  
GPP2\_RX0P  
GPP2\_RX0N

PCIE GPP2

GPP3\_RX9P  
GPP3\_RX9N  
GPP3\_RX8P  
GPP3\_RX8N  
GPP3\_RX7P  
GPP3\_RX7N  
GPP3\_RX6P  
GPP3\_RX6N  
GPP3\_RX5P  
GPP3\_RX5N  
GPP3\_RX4P  
GPP3\_RX4N  
GPP3\_RX3P  
GPP3\_RX3N  
GPP3\_RX2P  
GPP3\_RX2N  
GPP3\_RX1P  
GPP3\_RX1N  
GPP3\_RX0P  
GPP3\_RX0N

AF9  
AG9  
AG8  
AH8  
AF7  
AG7  
AG6  
AH6  
AG4  
AH4  
AE3  
AE2  
AC3  
AC2  
AB2  
AB1  
AA3  
AA2  
Y2  
Y1  
W3  
W2  
V2  
V1  
U3  
U2  
T2  
T1  
R3  
R2  
P2  
P1

EXP A\_TXP[0..15] &gt;&gt; EXP\_A\_TXP[0..15] 18

EXP A\_TXN[0..15] &gt;&gt; EXP\_A\_TXN[0..15] 18

EXP A\_RXP[0..15] &gt;&gt; EXP\_A\_RXP[0..15] 18

EXP A\_RXN[0..15] &gt;&gt; EXP\_A\_RXN[0..15] 18

AD11  
AC11  
AE12  
AD13  
AC13  
AD14  
AD15  
AC15  
AE16  
AD16  
AD17  
AC17  
AE18  
AD18  
AD19  
AC19  
AH20  
AG20

GPP3\_RX9P  
GPP3\_RX9N  
GPP3\_RX8P  
GPP3\_RX8N  
GPP3\_RX7P  
GPP3\_RX7N  
GPP3\_RX6P  
GPP3\_RX6N  
GPP3\_RX5P  
GPP3\_RX5N  
GPP3\_RX4P  
GPP3\_RX4N  
GPP3\_RX3P  
GPP3\_RX3N  
GPP3\_RX2P  
GPP3\_RX2N  
GPP3\_RX1P  
GPP3\_RX1N  
GPP3\_RX0P  
GPP3\_RX0N

PCIE GPP3

GPP3\_TX9P  
GPP3\_TX9N  
GPP3\_TX8P  
GPP3\_TX8N  
GPP3\_TX7P  
GPP3\_TX7N  
GPP3\_TX6P  
GPP3\_TX6N  
GPP3\_TX5P  
GPP3\_TX5N  
GPP3\_TX4P  
GPP3\_TX4N  
GPP3\_TX3P  
GPP3\_TX3N  
GPP3\_TX2P  
GPP3\_TX2N  
GPP3\_TX1P  
GPP3\_TX1N  
GPP3\_TX0P  
GPP3\_TX0N

AH10  
AG10  
AG11  
AE11  
AH12  
AG12  
AE13  
AH14  
AG14  
AG15  
AF15  
AH16  
AG16  
AG17  
AF17  
AH18  
AG18  
AG19  
AF19

PCI E slot TX need CAP close to slot side

GPP\_TX4P\_C NC6 0.1u/4X7R/16V/K

GPP\_TX4N\_C NC5 0.1u/4X7R/16V/K

GPP\_TX3P\_C NC6 0.1u/4X7R/16V/K

GPP\_TX3N\_C NC5 0.1u/4X7R/16V/K

GPP\_TX2P\_C NC6 0.1u/4X7R/16V/K

GPP\_TX2N\_C NC5 0.1u/4X7R/16V/K

GPP\_TX1P\_C NC2 0.1u/4X7R/16V/K

GPP\_TX1N\_C NC1 0.1u/4X7R/16V/K

GPP\_TX0P\_C NC11 0.1u/4X7R/16V/K

GPP\_TX0N\_C NC12 0.1u/4X7R/16V/K

GPP\_TX3P\_C NC14 0.1u/4X7R/16V/K

GPP\_TX3N\_C NC13 0.1u/4X7R/16V/K

GPP\_TX2P\_C NC15 0.1u/4X7R/16V/K

GPP\_TX2N\_C NC16 0.1u/4X7R/16V/K

GPP\_TX1P\_C NC18 0.1u/4X7R/16V/K

GPP\_TX1N\_C NC17 0.1u/4X7R/16V/K

GPP\_TX0P\_C NC11 0.1u/4X7R/16V/K

GPP\_TX0N\_C NC12 0.1u/4X7R/16V/K

AC21  
AD21  
AE22  
AF25  
AG25  
AG26  
AH26

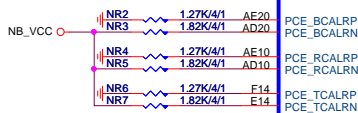
SB\_RX3P  
SB\_RX3N  
SB\_RX2P  
SB\_RX2N  
SB\_RX1P  
SB\_RX1N  
SB\_RX0P  
SB\_RX0N

PCIE ALINK

SB\_TX3P  
SB\_TX3N  
SB\_TX2P  
SB\_TX2N  
SB\_TX1P  
SB\_TX1N  
SB\_TX0P  
SB\_TX0N

AG22  
AH22  
AF21  
AG21  
AF23  
AG23  
AG24  
AH24

PLACE THESE CAP CLOSE TO NB.

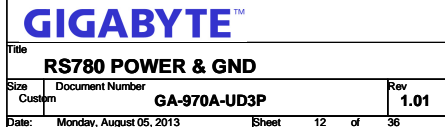


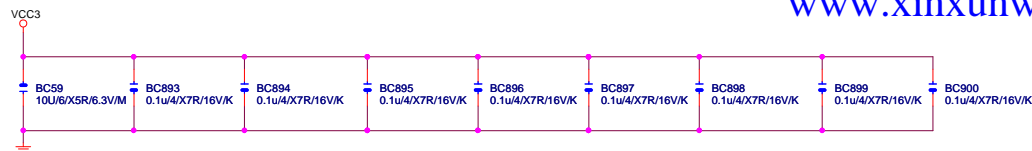
RX980/BGA692

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Title  
RS780 PCIE I/F ,SwitchSize  
Custom Document Number  
GA-970A-UD3PRev  
1.01

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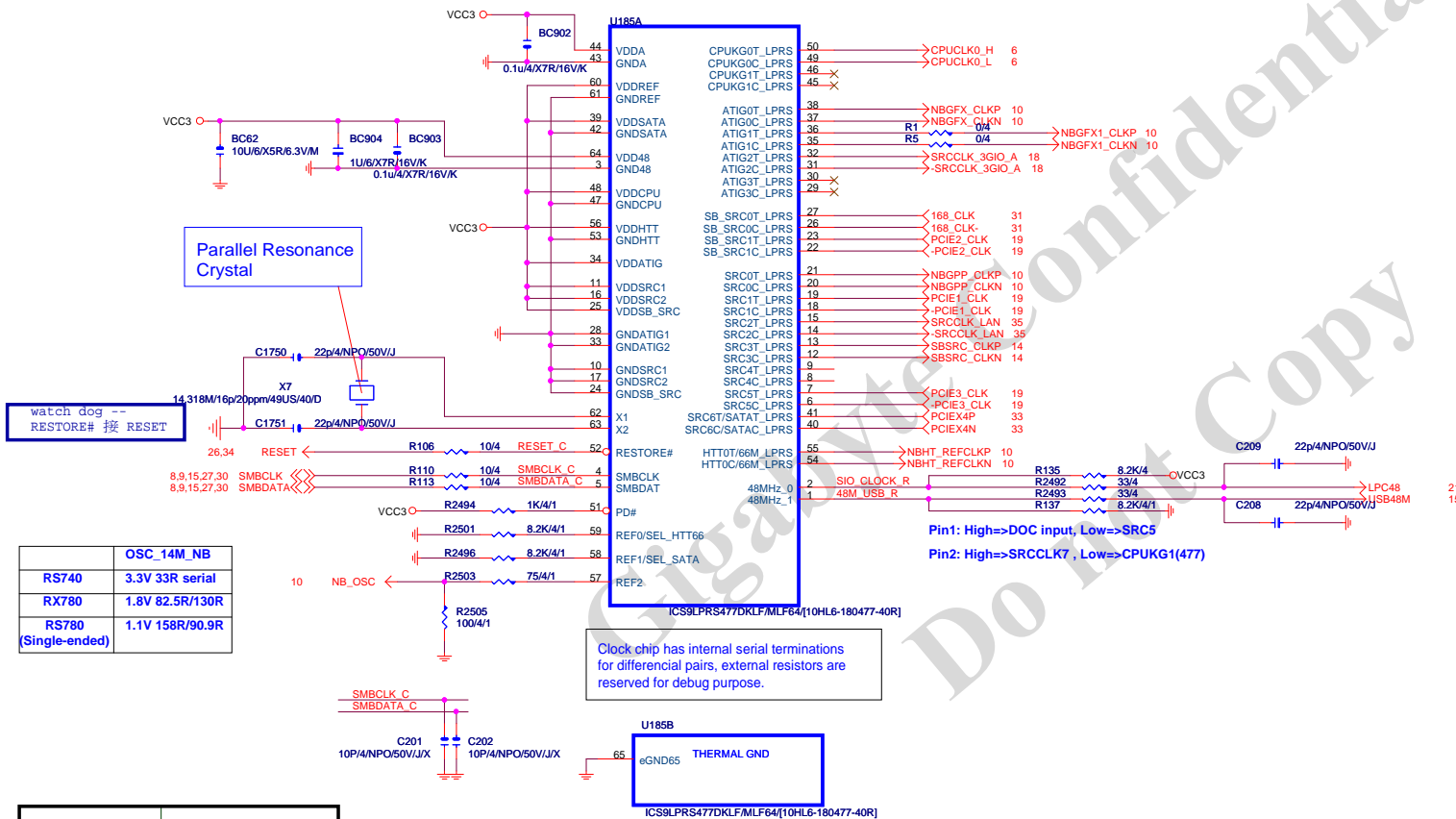


- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO U800 AS POSSIBLE
- 2- ROUTE ALL SRCCLKTx AND SRCCLKCx AS DIFFERENT PAIR RULE
- 3- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN

NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE (SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P				
REFCLK_N	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
	NC	NC	vref	100M DIFF
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF	
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPSSB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

\* the GFX\_REFCLK input is required for all cases

Place R800/801 less than 500 mils away from U800  
R851 less than 100 mils away from R800/801  
route CPU clock as 100ohm differential pair



	OSC_14M_NB
RS740	3.3V 33R serial
RX780	1.8V 82.5R/130R
RS780 (Single-ended)	1.1V 158R/90.9R

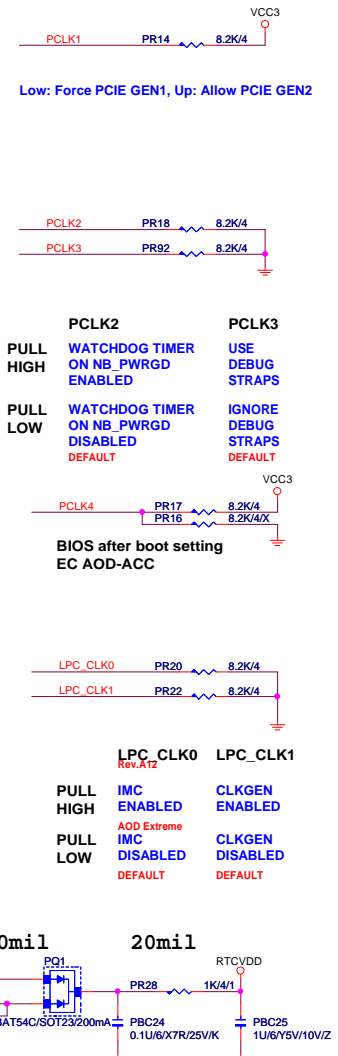
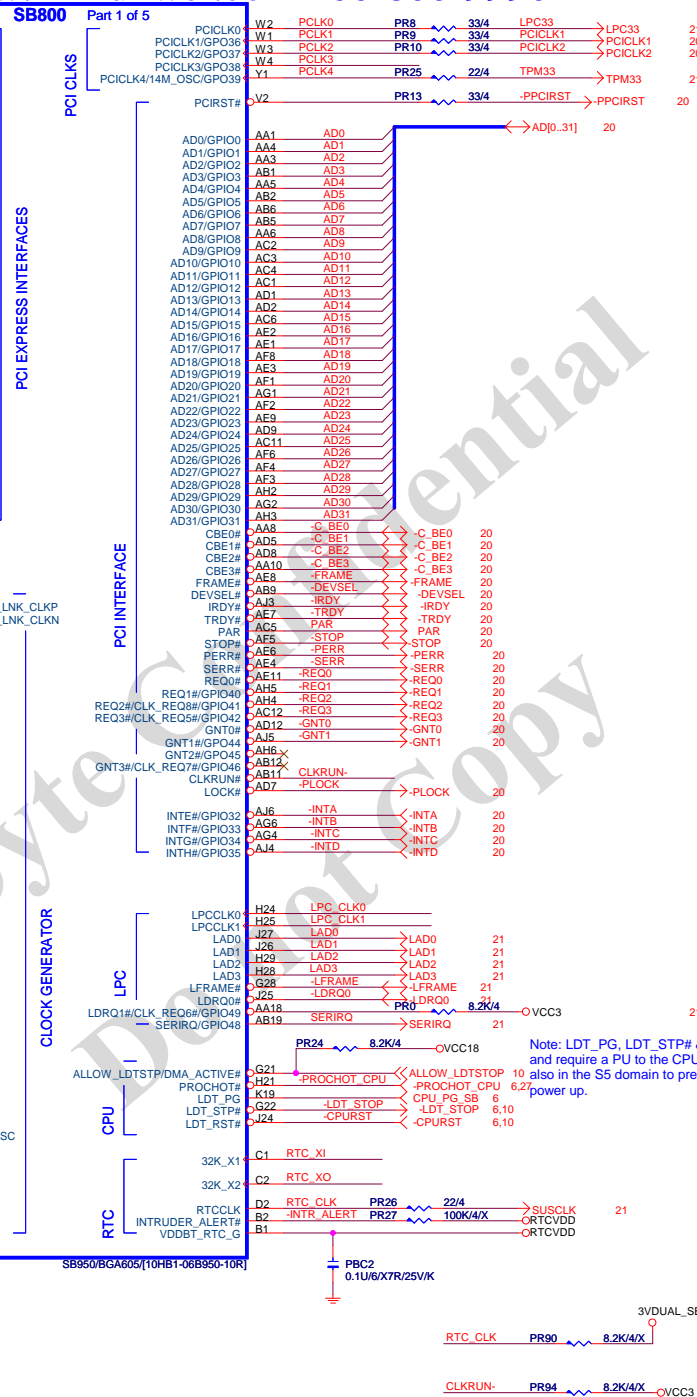
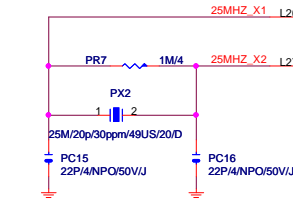
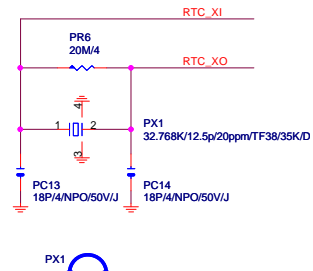
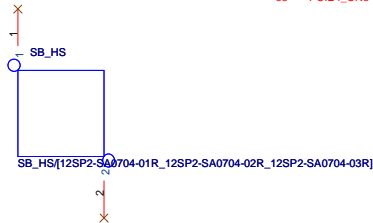
REF0/SEL_HTT66	HTT CLOCK
0	100.00 DIFFERENTIAL
1	66.66 SINGLE END

REF1/SEL_SATA	SRC6/SATA
0	100.00 DIFFERENTIAL SPREADING SRC CLOCK
1	100.00 NON-SPREADING DIFFERENTIAL SATA CLOCK

<b>GIGABYTE™</b>			
Title <b>RTM880N-793</b>			
Size Customer	Document Number <b>GA-970A-UD3P</b>		Rev <b>1.01</b>
Date:	Monday, August 05, 2013	Sheet 13 of 36	

PLACE THESE PCIE AC COUPLING CAPS CLOSE TO SB850

**S.B HEATSINK**



CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL

**NOT ADD ICT FOR RTCVDD PIN**

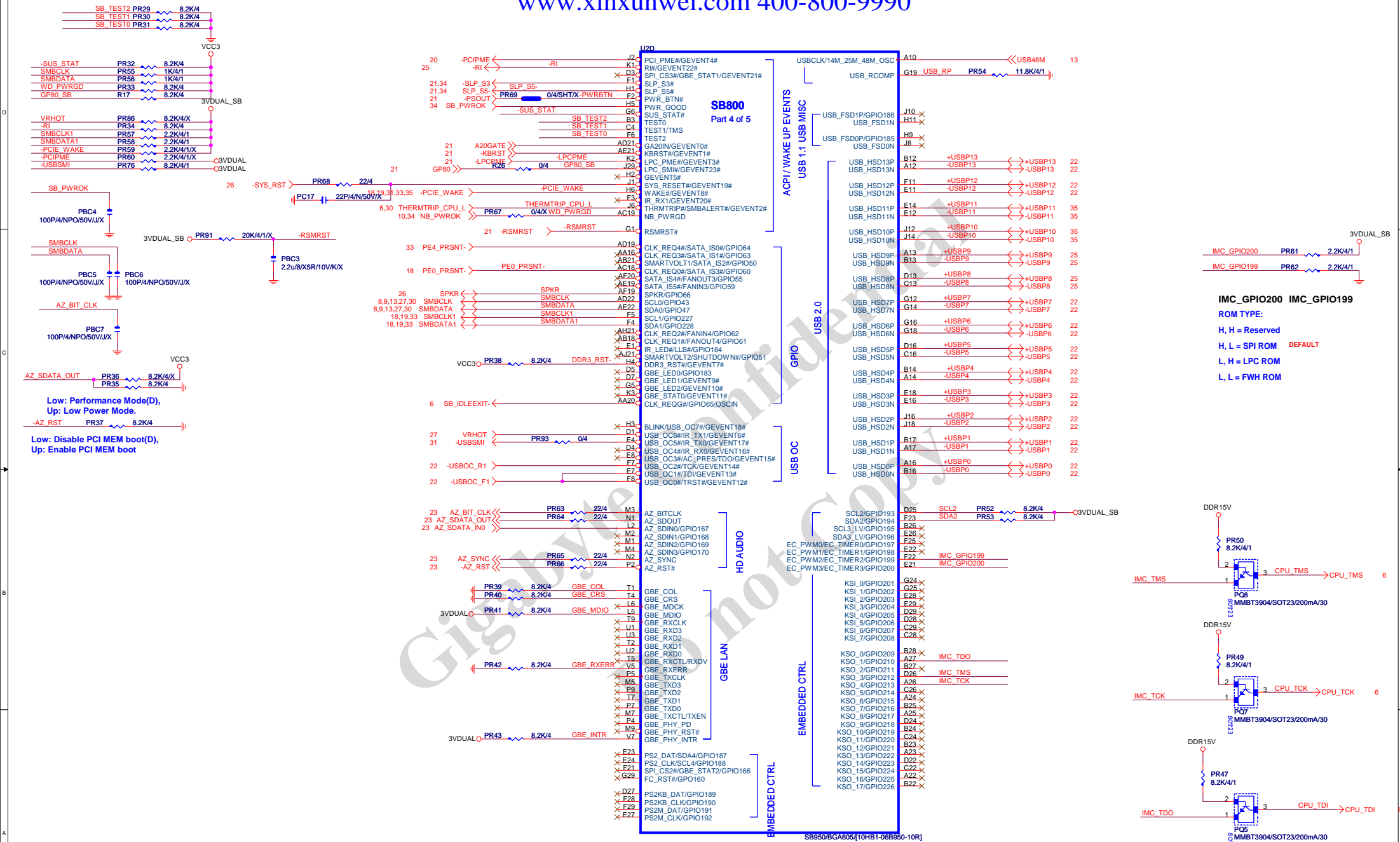
**GIGABYTE**

Title  
**ATI SB700 PCIE/PC/CPU/LPC**

Size	Document Number	Rev
Custom	GA-970A-UD3P	1.01

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GIGABYTE™

ATI SB700 ACPI/USB/GPIO/AUDIO

Size Custom Document Number GA-970A-UD3P Rev 1.01

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PLACE SATA CAL  
RES VERY CLOSE  
TO BALL OF U600

# NOTE:

R650 IS 1K 1% FOR 25MHz  
XTAL, 4.99K 1% FOR 100MHz  
INTERNAL CLOCK

VCC\_SB C PR75 1K/4/1 SATA\_CALRP AB14  
PR74 931/4/1 SATA\_CALRN AA14

26 -SATA\_LED -SATA\_LED AD11

TP5 SATA\_X1 AD16

TP7 SATA\_X2 AC16

SB SPI DI PR70 22/4 SB SPI DI R J5  
SB SPI DO PR71 22/4 SB SPI DO R E2  
SB SPI CLK PR72 22/4 SB SPI CLK R K4  
SB SPI CS\_ITE PR73 22/4 SB SPI CS\_ K9  
21 -SB\_SPI\_CS\_ITE X G2

SATA

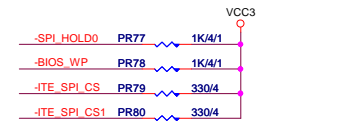
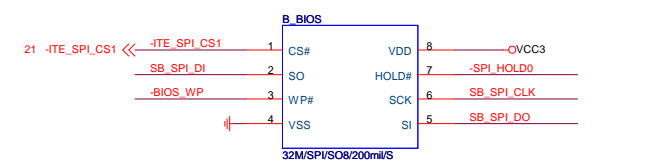
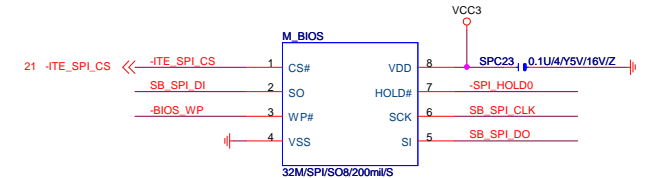
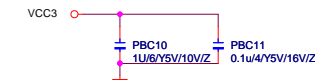
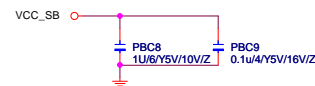
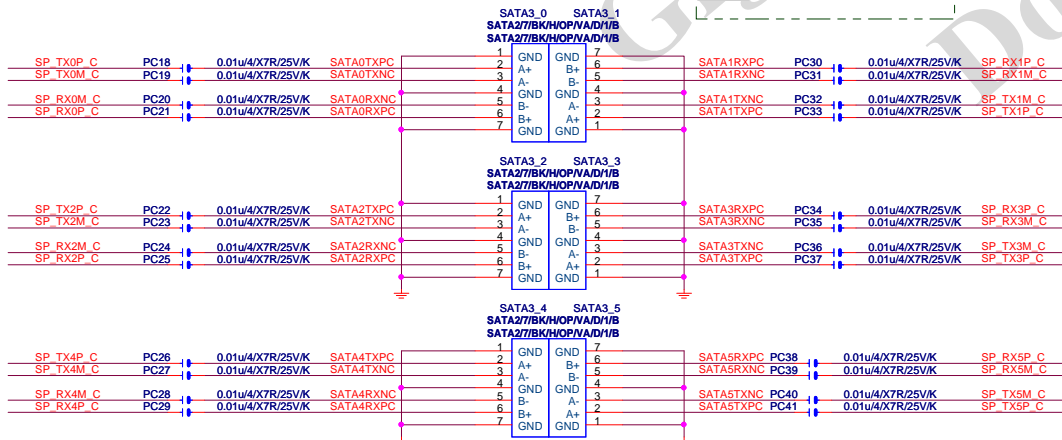
HW MONITOR

SPIROM

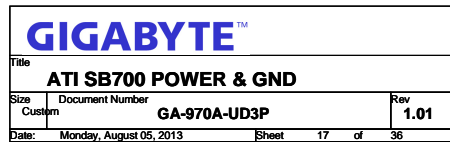
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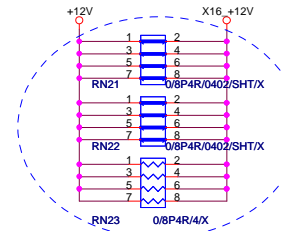
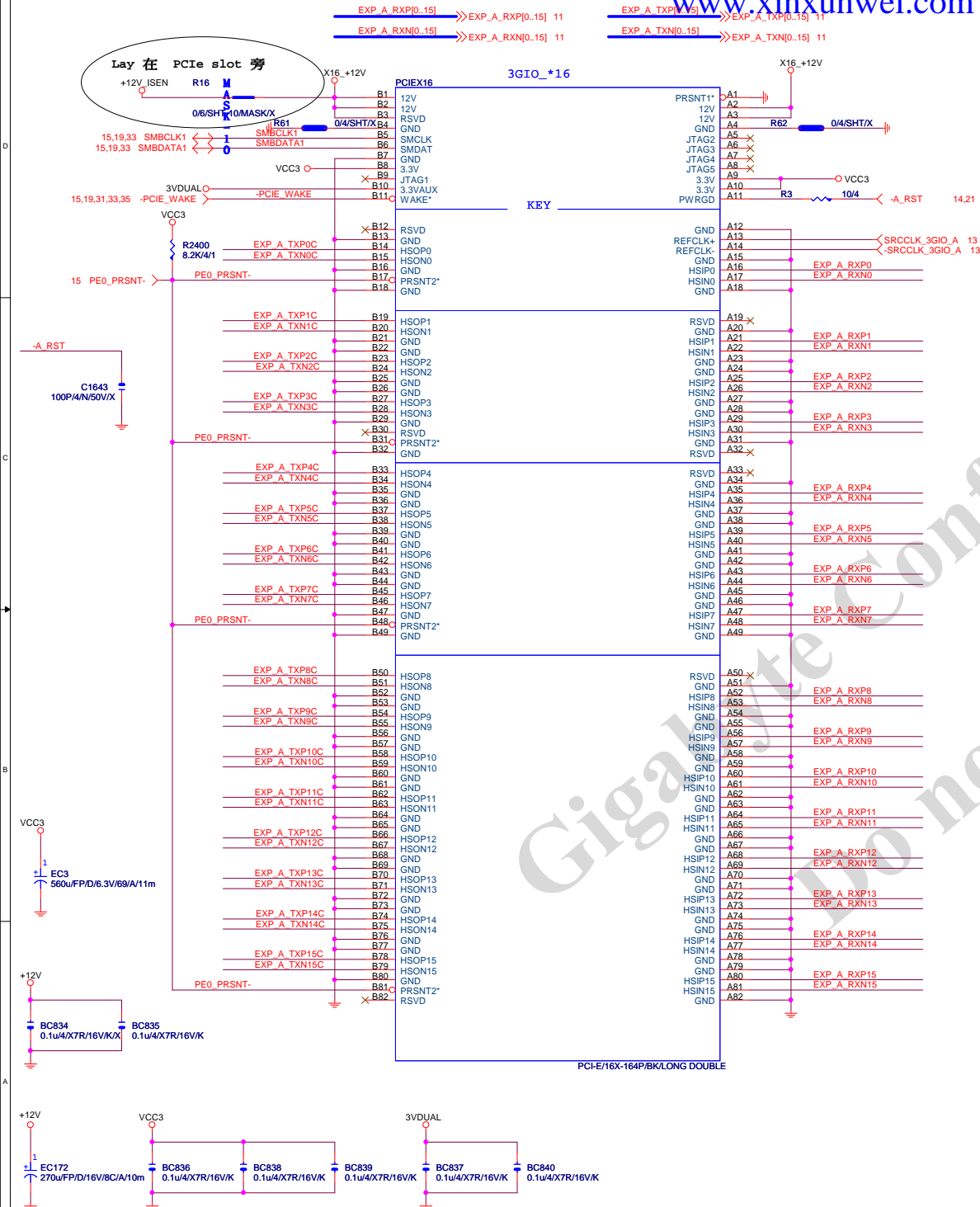


PLACE SATA AC COUPLING  
CAPS CLOSE TO SB850

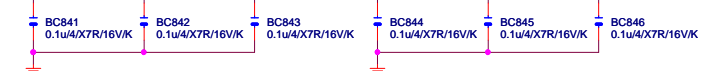
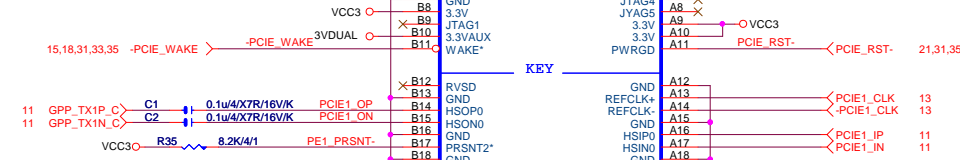


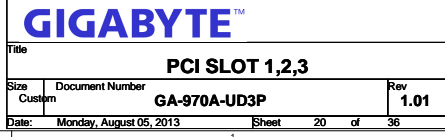
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Size Custom	Document Number GA-970A-UD3P	Rev 1.01
Date Monday, August 05, 2013	Sheet 16	of 36

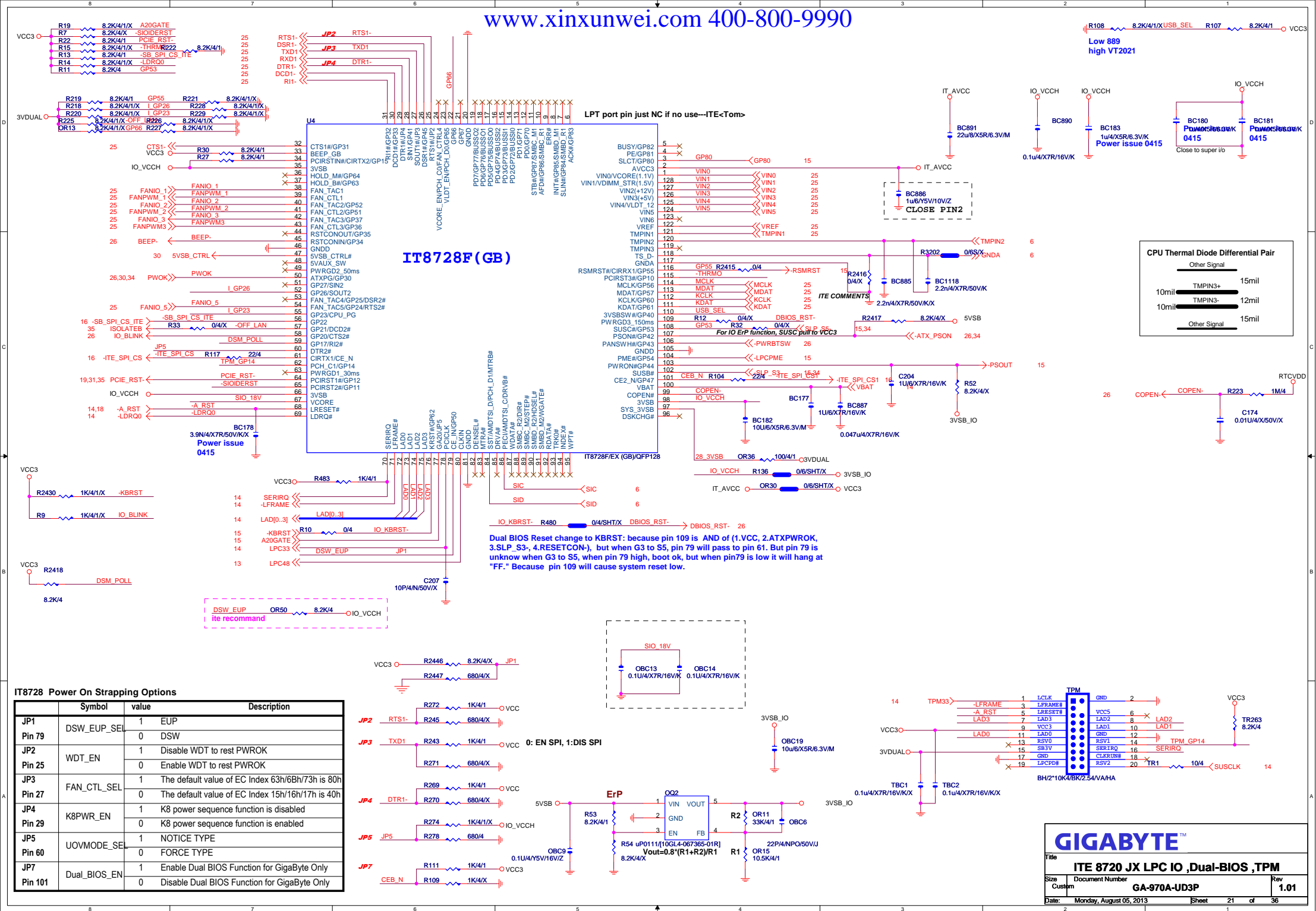




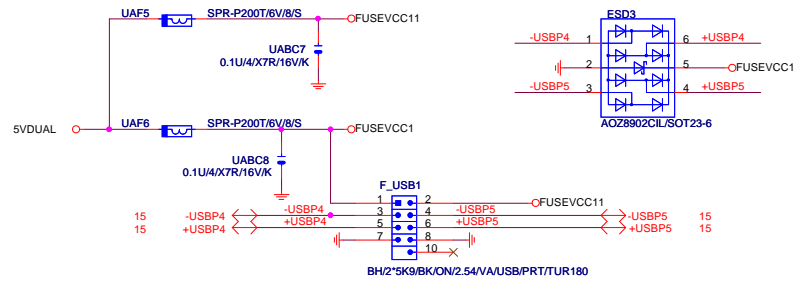
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EXP A TXN0	C1645	0.1u4/4X7R/16V/K	EXP A TXN0C
EXP A TXP1	C1646	0.1u4/4X7R/16V/K	EXP A TXP1C
EXP A TXN1	C1647	0.1u4/4X7R/16V/K	EXP A TXN1C
EXP A TXP2	C1648	0.1u4/4X7R/16V/K	EXP A TXP2C
EXP A TXN2	C1649	0.1u4/4X7R/16V/K	EXP A TXN2C
EXP A TXP3	C1650	0.1u4/4X7R/16V/K	EXP A TXP3C
EXP A TXN3	C1651	0.1u4/4X7R/16V/K	EXP A TXN3C
EXP A TXP4	C1652	0.1u4/4X7R/16V/K	EXP A TXP4C
EXP A TXN4	C1653	0.1u4/4X7R/16V/K	EXP A TXN4C
EXP A TXP5	C1654	0.1u4/4X7R/16V/K	EXP A TXP5C
EXP A TXN5	C1655	0.1u4/4X7R/16V/K	EXP A TXN5C
EXP A TXP6	C1656	0.1u4/4X7R/16V/K	EXP A TXP6C
EXP A TXN6	C1657	0.1u4/4X7R/16V/K	EXP A TXN6C
EXP A TXP7	C1658	0.1u4/4X7R/16V/K	EXP A TXP7C
EXP A TXN7	C1659	0.1u4/4X7R/16V/K	EXP A TXN7C
EXP A TXP8	C1660	0.1u4/4X7R/16V/K	EXP A TXP8C
EXP A TXN8	C1661	0.1u4/4X7R/16V/K	EXP A TXN8C
EXP A TXP9	C1662	0.1u4/4X7R/16V/K	EXP A TXP9C
EXP A TXN9	C1663	0.1u4/4X7R/16V/K	EXP A TXN9C
EXP A TXP10	C1664	0.1u4/4X7R/16V/K	EXP A TXP10C
EXP A TXN10	C1665	0.1u4/4X7R/16V/K	EXP A TXN10C
EXP A TXP11	C1666	0.1u4/4X7R/16V/K	EXP A TXP11C
EXP A TXN11	C1667	0.1u4/4X7R/16V/K	EXP A TXN11C
EXP A TXP12	C1668	0.1u4/4X7R/16V/K	EXP A TXP12C
EXP A TXN12	C1669	0.1u4/4X7R/16V/K	EXP A TXN12C
EXP A TXP13	C1670	0.1u4/4X7R/16V/K	EXP A TXP13C
EXP A TXN13	C1671	0.1u4/4X7R/16V/K	EXP A TXN13C
EXP A TXP14	C1672	0.1u4/4X7R/16V/K	EXP A TXP14C
EXP A TXN14	C1673	0.1u4/4X7R/16V/K	EXP A TXN14C
EXP A TXP15	C1674	0.1u4/4X7R/16V/K	EXP A TXP15C
EXP A TXN15	C1675	0.1u4/4X7R/16V/K	EXP A TXN15C



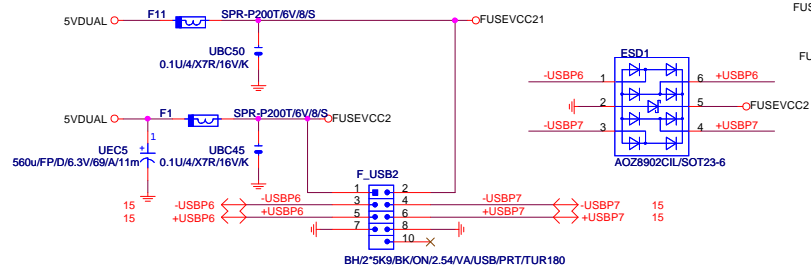




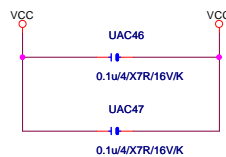
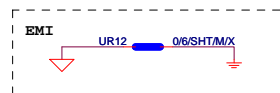
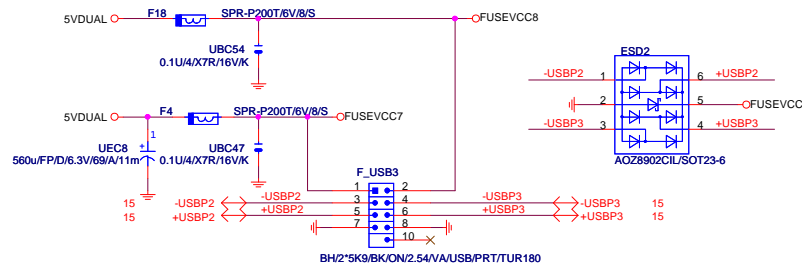
## FRONT SIDE USB1



## FRONT SIDE USB2

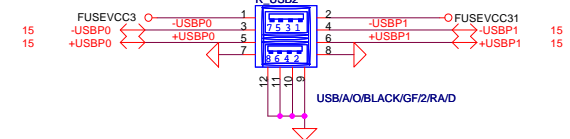
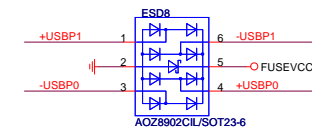
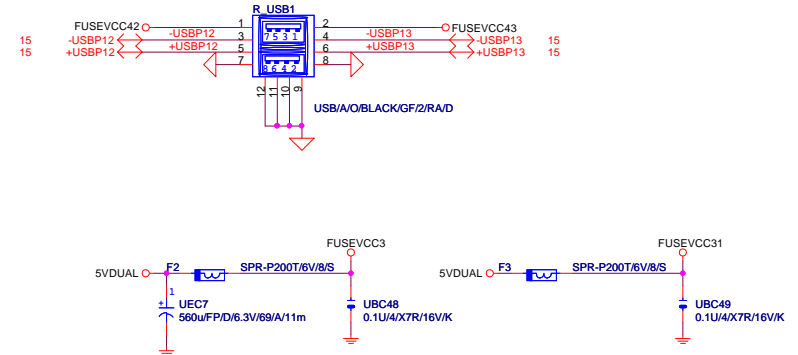
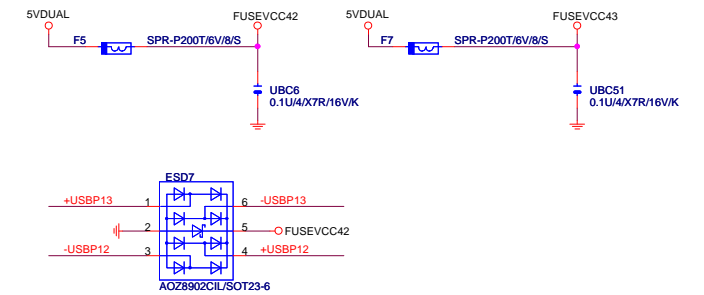


## FRONT SIDE USB3



Please close 前後窗各一顆USB3.0

## REAR USB



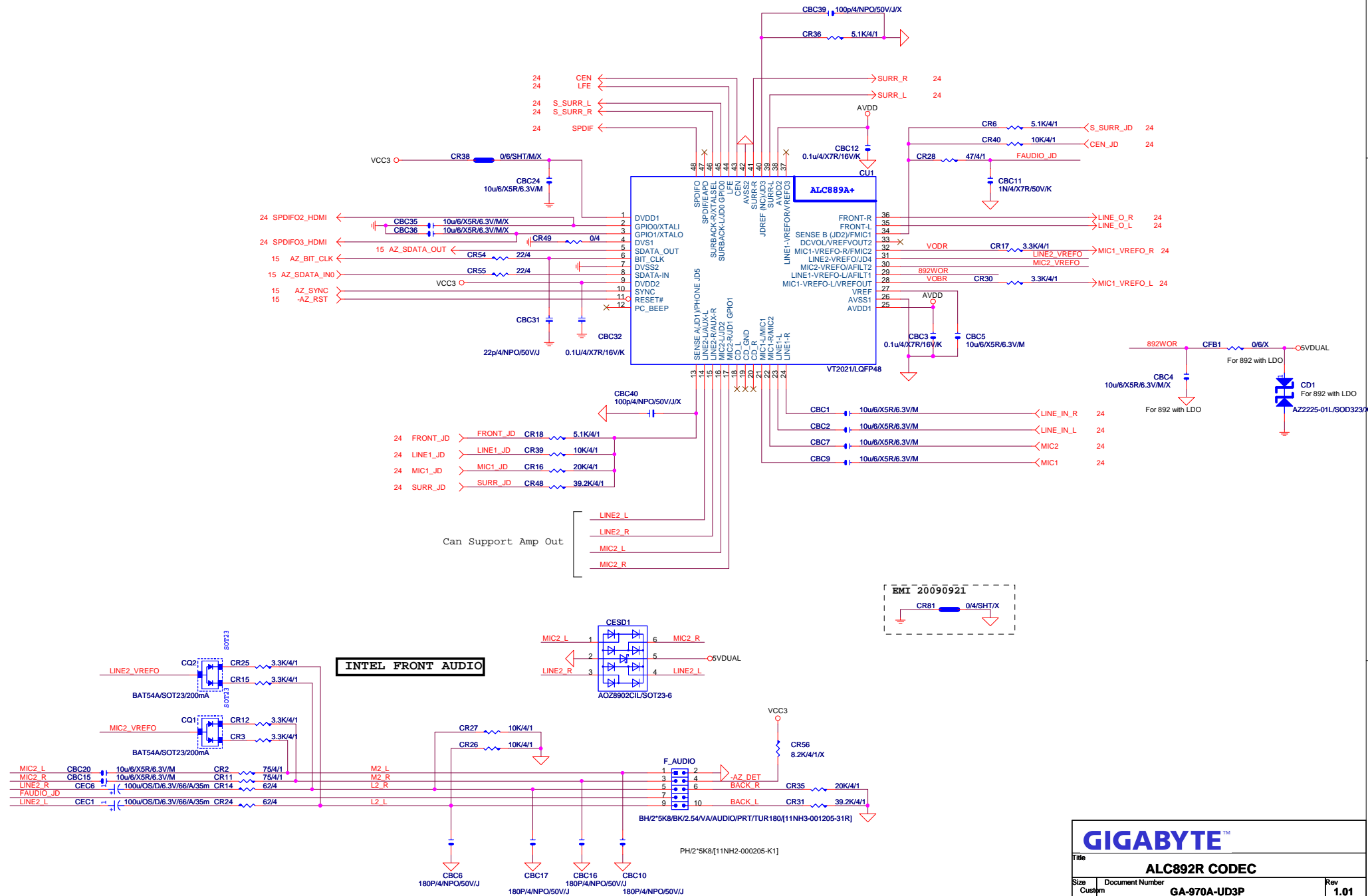
GIGABYTE™

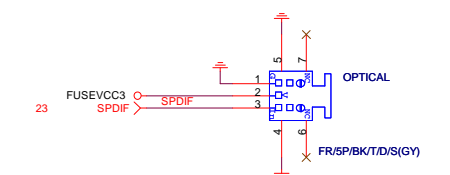
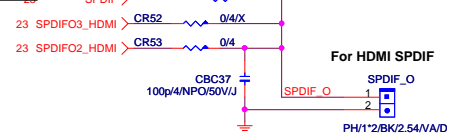
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Size Custom Document Number GA-970A-UD3P Rev 1.01

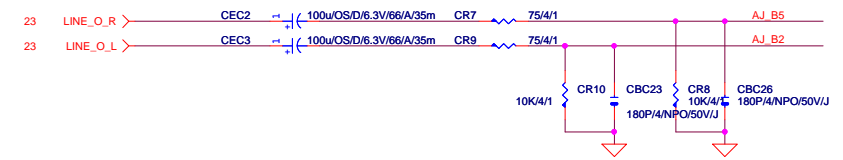
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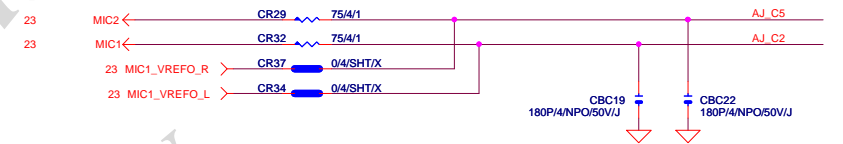
LINE OUT  
FRONT OUT



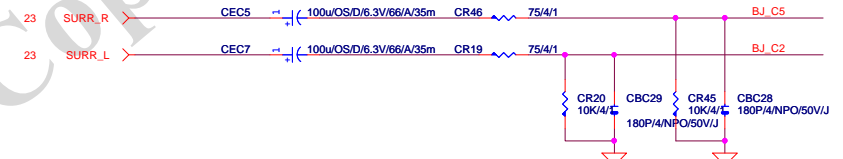
LINE-IN



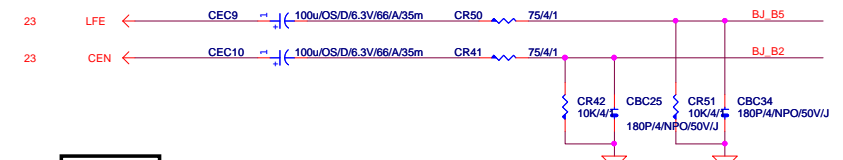
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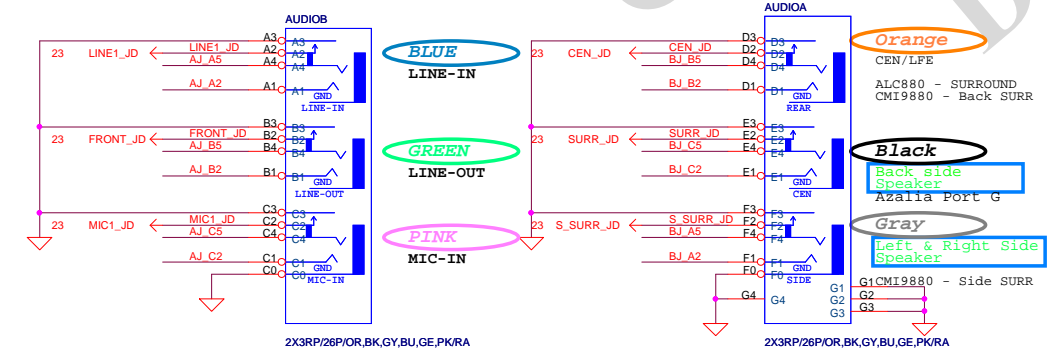
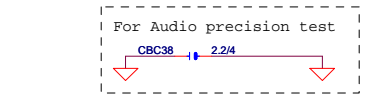
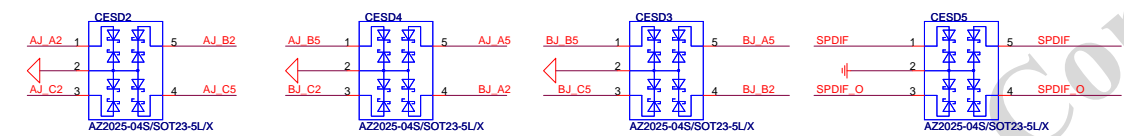
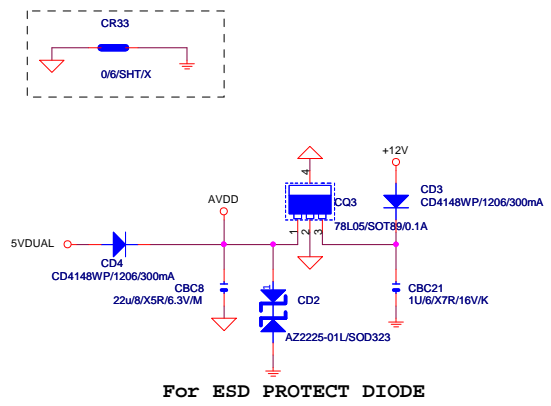
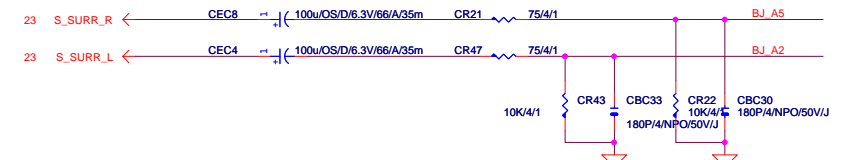
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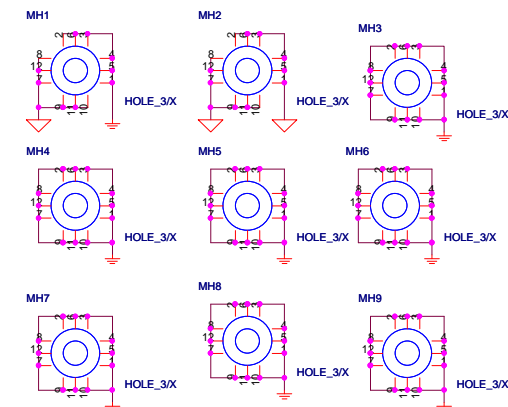
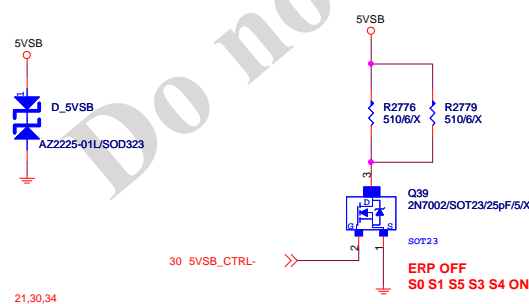
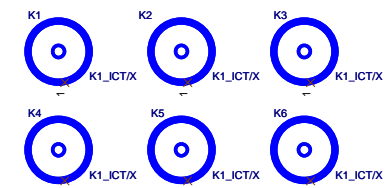
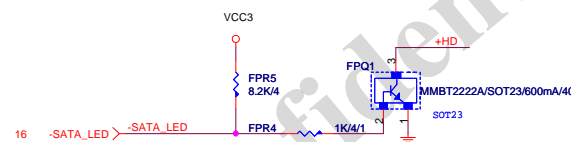
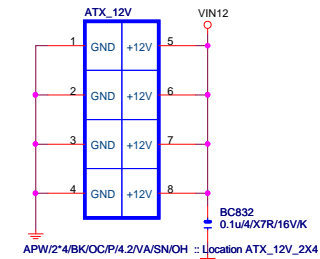
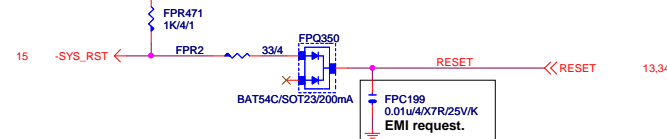
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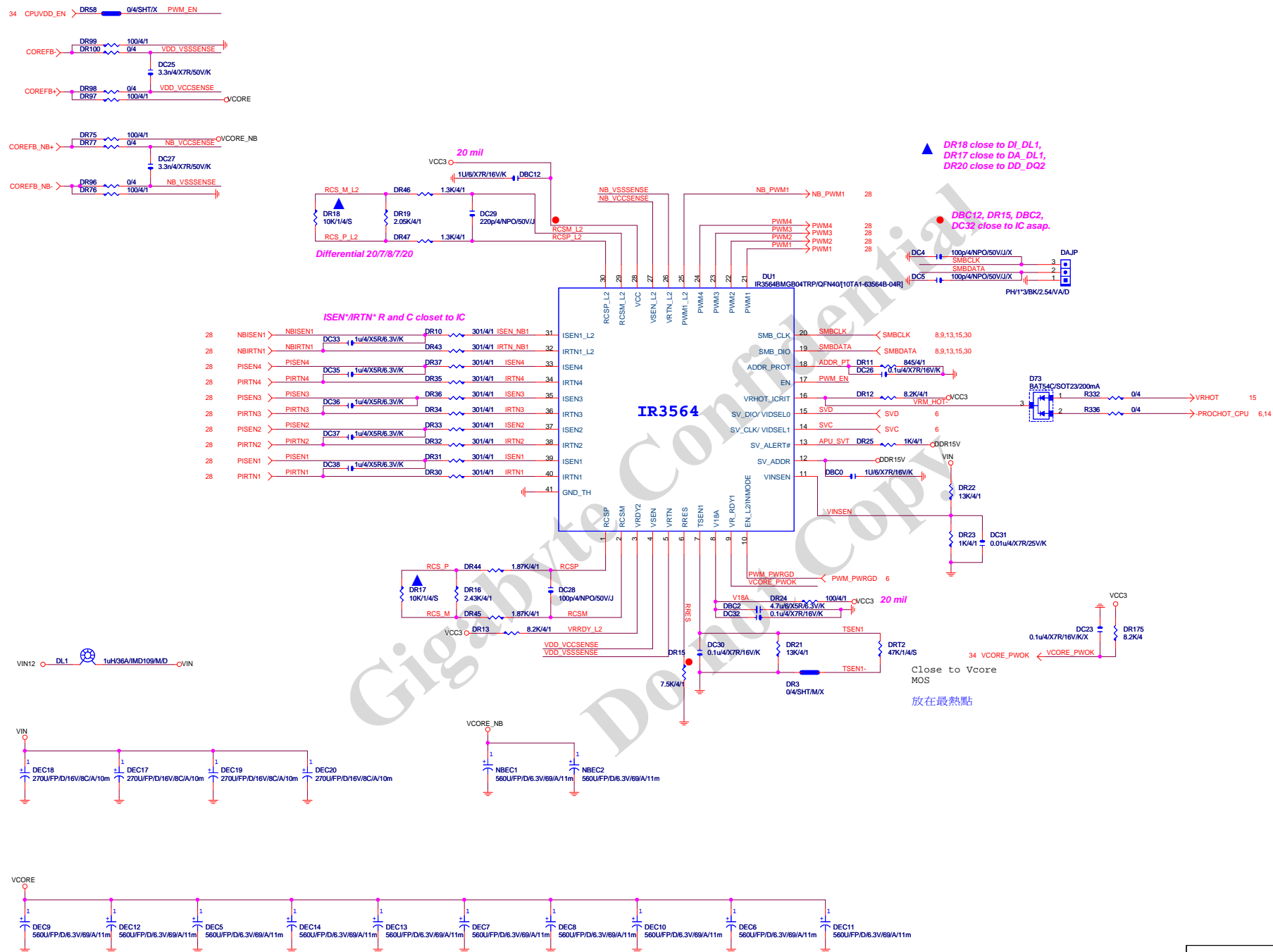


SURR BACK







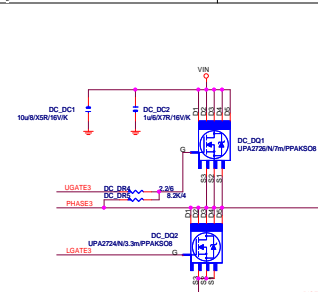


GIGABYTE™

Title: Vcore (Pwm) ISL6324A+6612A)

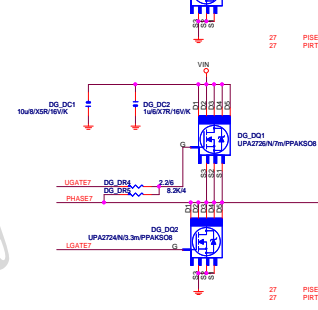
Size: Custom Document Number: GA-970A-UD3P Rev: 1.01

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FUNCTION	MODE	FROM MODE	PHASE MODE
0	1	IR ATL	DUAL
1	1	IR ATL	Doubler
0	0	Tri-Sate	DUAL
1	0	Tri-Sate	Doubler
OPEN	0	Tri-Sate	Quad
OPEN	1	IR ATL	Quad

In Quad mode , IC1 pin10 link to IC2 pin10  
IC1 pin9 link to IC2 pin9 without FU

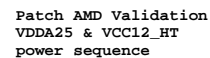
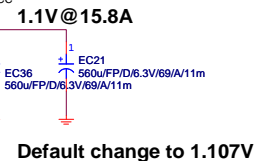


FUNCTION	MODE	PWM MODE	PHASE MODE
0	1	IR ATL	DCAL
1	1	IR ATL	Doubler
0	0	Tri-Sense	DCAL
1	0	Tri-Sense	Doubler
OPEN	0	Tri-Sense	Quad

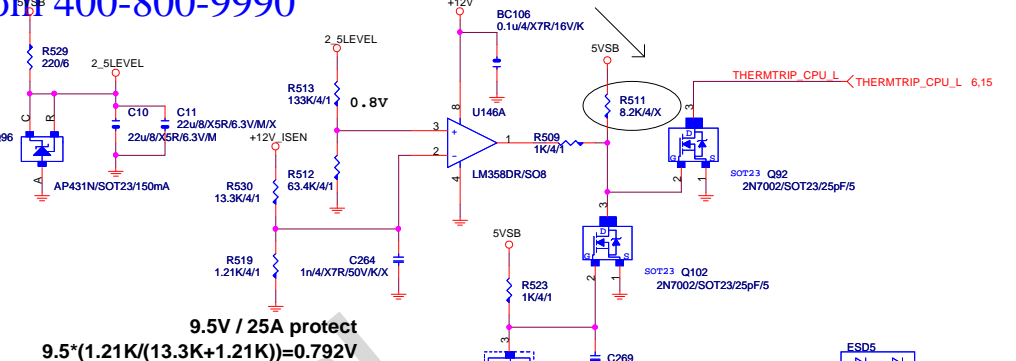
OPEN	1	IR ATL	Quad
------	---	--------	------

In Quad mode , IC1 pin10 link to IC2 pin10

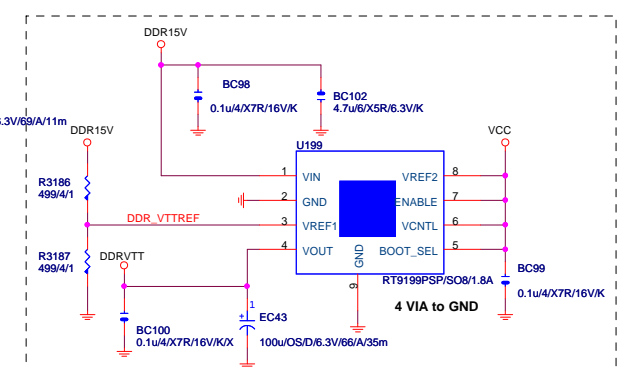
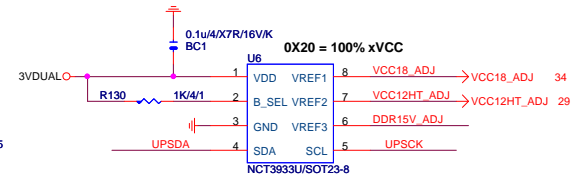
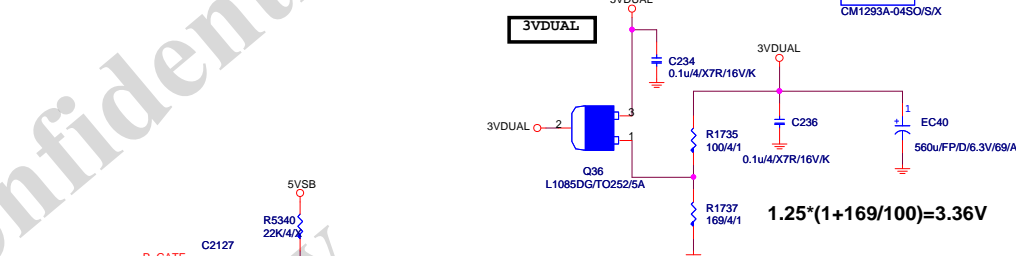



$$1.25 \times (1 + 100/100) = 2.5V$$



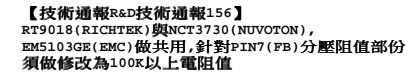
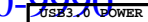


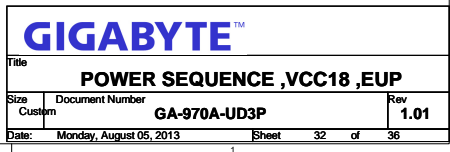
Pin configuration diagram for the CM1293A-04SO/S/X component. The component is shown in a 4-pin package. Pin 1 is labeled 'E5D5'. Pin 2 is labeled '3V3DUAL'. Pin 3 is labeled 'SMBCLK'. Pin 4 is labeled 'SMBDATA'.



Title			
<b>DDR POWER</b>			
Size	Document Number	Rev	
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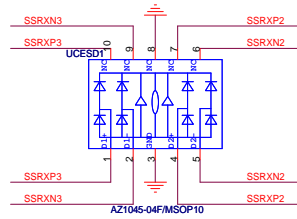
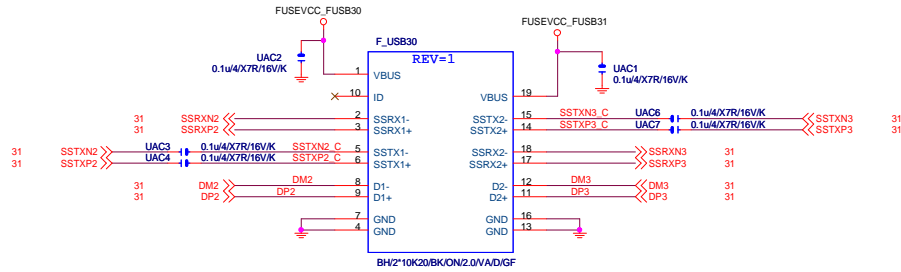
## VL805



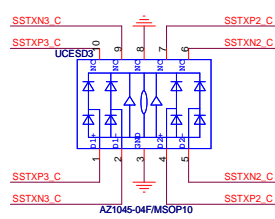




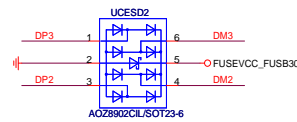
## FRONT SIDE USB3



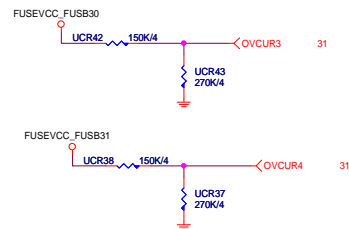
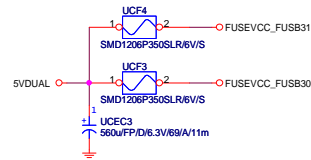
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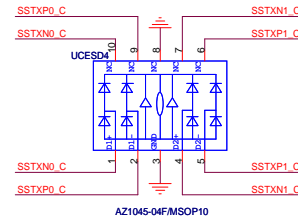
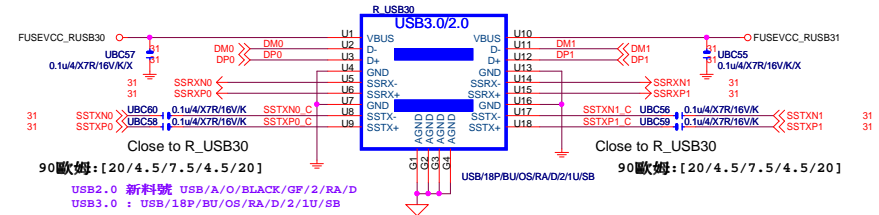
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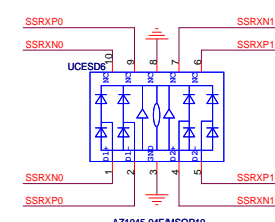
Close to connector



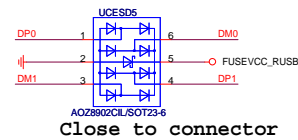
## REAR SIDE USB3



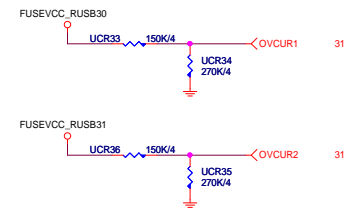
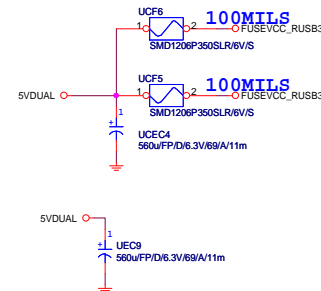
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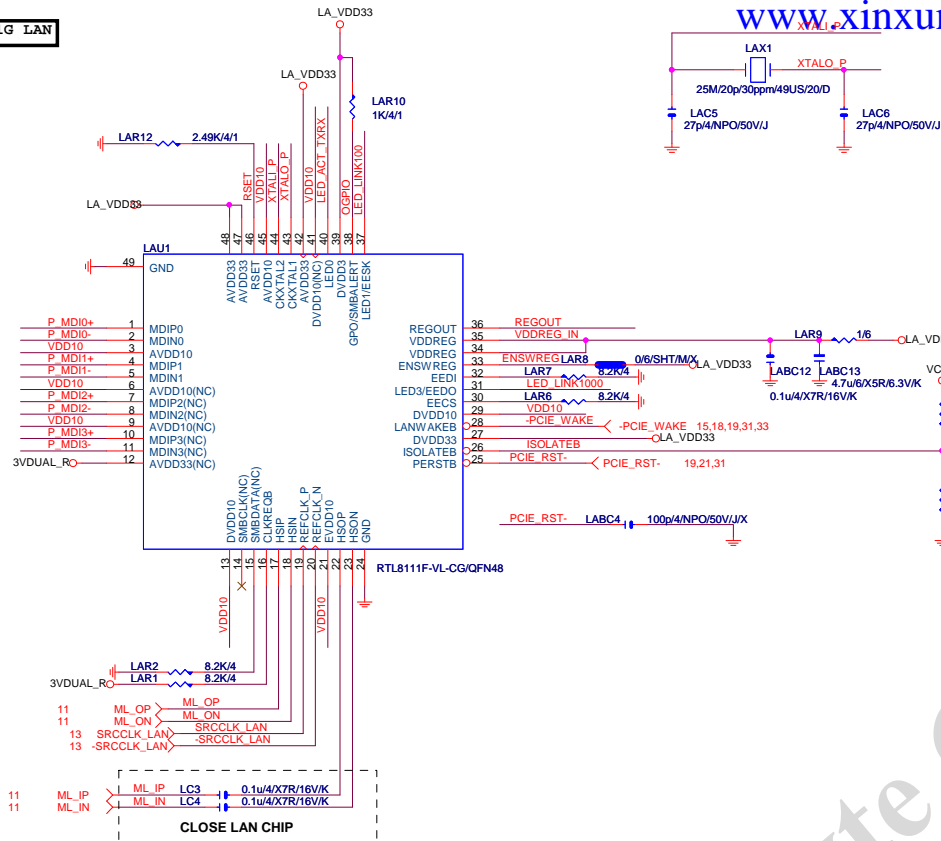
Close to connector



Close to connector

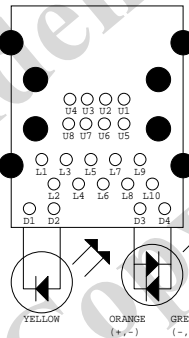


## PCIE-1G LAN



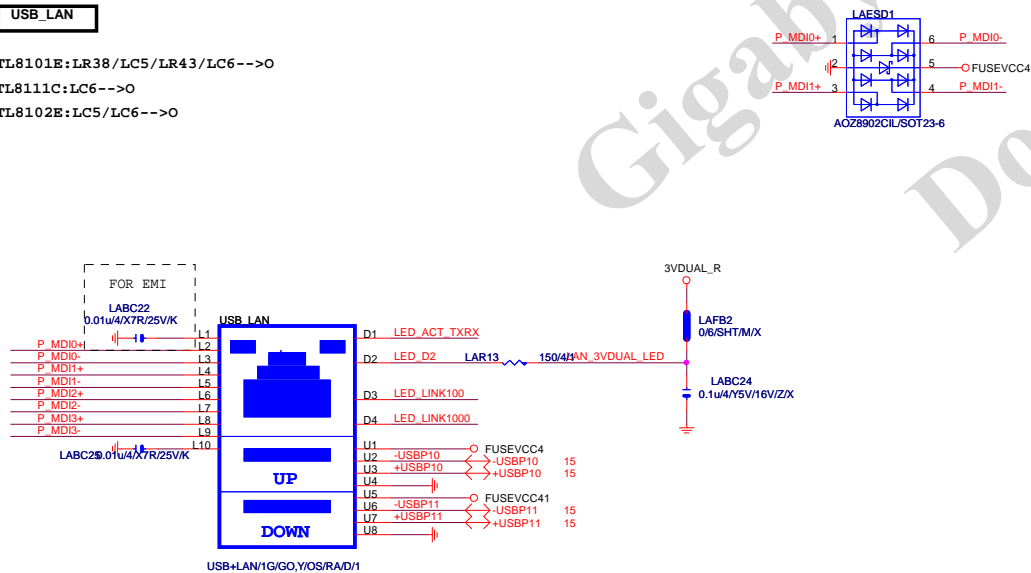
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P35-152-19W9

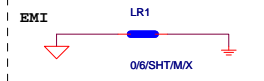


## USB LAN

RTL8101E:LR38/LC5/LR43/LC6--->O  
 RTL8111C:LC6--->O  
 RTL8102E:LC5/LC6--->O



RTL8101E :L1+L10-->AVDD18+0.1U(BIOS DISABLE MDI-X FUNCTION)  
 1G :USB+LAN/1G/GO,Y/OS/RA/D/1  
 100M:USB+LAN/100/GO,Y/OS/RA/D/1



GIGABYTE

REALTK RTL8111C

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